WHAT IS CLAIMED IS:

1. A die test apparatus comprising:

a plurality of dice fabricated on a wafer

a common signal line for applying a signal in common to said plurality of dice; and

a plurality of temporary isolation devices respectively provided between said common signal line and said plurality of dice, each said temporary isolation device permitting an associated die to be temporarily disconnected from said common signal line.

2. An apparatus of claim 1 wherein said temporary isolation device is a unidirectional current device.

3. An apparatus of claim 2 wherein said temporary isolation device is a diode.

4. An apparatus of claim 2 wherein said temporary isolation device is a transistor.

5. An apparatus of claim 4 wherein said transistor is connected as a diode.

6. An apparatus of claim 4 wherein said transistor is connected to be controlled by an applied signal.

7. An apparatus of claim 1 wherein said common signal line supplies a power supply signal to said dice.

8. An apparatus of claim 1, further comprising a plurality of permanent isolation devices respectively provided in series with said plurality of temporary isolation devices, each said permanent isolation device being capable of providing permanent isolation between said common signal line and a respective die.

9. An apparatus of claim 8, wherein each said permanent isolation devices comprises a fuse.

10. An apparatus of claim 1 wherein said common signal line is provided on said wafer.

11. An apparatus of claim 1 further comprising an external interface for testing said plurality of dies and wherein said common signal line is provided on said external interface.

12. An apparatus of claim 1 wherein each said temporary isolation device is provided off an associated die.

13. An apparatus of claim 12 wherein each said temporary isolation device is provided on said wafer.

14. An apparatus of claim 13 wherein each said temporary isolation device is provided in a street area of said wafer.

15. An apparatus of claim 12 wherein each said temporary isolation device is provided at an external interface for testing said plurality of dies.

16. An apparatus of claim 1 wherein each temporary isolation device is provided on a respective die.

17. An apparatus of claim 8 wherein each said permanent isolation device is provided off a respective die.

18. An apparatus of claim 17 each said permanent isolation device is provided on said wafer.

19. An apparatus of claim 18 each said permanent isolation device is provided in a street area of said wafer.

20. An apparatus of claim 17 where each said permanent isolation device is provided at an external interface for testing said plurality of dies.

21. An apparatus of claim 8, wherein each permanent isolation device is provided on a respective die.

22. An apparatus of claim 1 further comprising a pair of shortable spaced terminals in an electrical path between each said die and said common conductor.

23. An apparatus of claim 22 wherein a first one of said spaced terminals is provided on a said die and a second one of said terminals is provided off said die.

24. An apparatus of claim 23 wherein said second one of said terminals is provided in a street area of said wafer.

25. A semiconductor wafer comprising:

a first signal line provided along said wafer for supplying a first signal;

a plurality of dice fabricated on said wafer, each comprising an integrated circuit and a first terminal used to apply a first signal to internal components of said die; and

a plurality of unidirectional circuit devices, each coupled between said first common conducting line and a first terminal of a respective die for allowing a signal to move in only one direction between said first line and the first terminal of a respective die.

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26. A wafer of claim 25 wherein said unidirectional circuit devices are provided on a respective dice.

27. A wafer of claim 25 wherein said unidirectional circuit devices are provided off a respective dice.

28. A wafer of claim 25 further comprising a plurality of permanent isolation devices respectively interposed between said signal line and each said die.

29. A wafer of claim 28 wherein said permanent isolation devices are respectively provided on said dice.

30. A wafer of claim 28 wherein said permanent isolation devices are provided off said dice.

31. A wafer of claim 25 wherein each unidirectional circuit device is a diode.

32. A wafer of claim 25 wherein each unidirectional circuit device is a transistor.

33. A wafer of claim 25 wherein the first signal line comprises a power supply line.

34. A semiconductor wafer comprising:

a plurality of individual dice containing respective integrated circuits;

at least a first signal conductor provided on said wafer for supplying at least a first voltage to each die;

each die comprising:

circuitry for performing an electrical function; and

a temporary isolation device connected between said first signal conductor and said circuitry for temporarily isolating said circuitry from said first conductor.

35. A wafer of claim 34 wherein said temporary isolation device is a diode.

36. A wafer of claim 34 wherein said temporary isolation device is a transistor.

37. A method of testing a plurality of dice fabricated on a wafer, said method comprising:

connecting a first terminal of each of said plurality of dice to a common signal conductor through respective temporary isolation devices which allow said dice to receive a signal from said common signal conductor during a first test procedure; and connecting said first terminal of at least some of said plurality of dice to another conductor during a second test procedure, said temporary isolation devices being activated during said second test procedure to isolate said first terminal of said at least some of said dice from said common signal conductor during said second test procedure.

38. A method of testing a semiconductor die on a wafer comprising:

(1) applying voltage to a first voltage line which connects with a plurality of dice on said wafer through respective temporary isolation devices;

(2) removing voltage from said first voltage line; and

(3) applying voltage to a die by connecting a probe to a first voltage terminal associated with said die, said die being isolated from said first voltage line by a respective temporary isolation device.

39. A method of claim 38 wherein steps (1) and (2) are performed before step (3).

40. a method of claim 37 further comprising permanently isolating a die from said common first voltage conductor as a result of tests performed in said first or second test procedure.

41. A method of claim 38 wherein step (1) is performed after steps (2) and (3).

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